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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,247	06/20/2003	K. Naresh Chandra Srinivas	14974US01	5550

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MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
HUYNH, KIM NGOC	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,247	SRINIVAS ET AL.	
	Examiner	Art Unit	
	Kim Huynh	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10 and 17-20* is/are rejected.

7)☒ Claim(s) *5-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-10 and 17-20, drawn to input/output command process, classified in class 710, subclass 5.

   II. Claims 11-16, drawn to input/output process timing, classified in class 710, subclass 58.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the logic as claim in the apparatus does not required timing relationship timing relationship of the process.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

3. During a telephone conversation with Mr. Mirut P. Dalal, on 11/15/04, a provisional election was made without traverse to prosecute the invention of group I, claims 1-10 and 17-20. Affirmation of this election must be made by applicant in

replying to this Office action. Claims 11-16 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 3 and 17-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 17 recites the first printed circuits connecting to the memory controller and the memory module and a second printed circuit connected to the memory module and the logic. The specification fails to provide support to a first and second printed circuit board connected as claimed. At best the specification, in paragraph 31, discloses the

memory controller and the memory module are implemented as separate integrated circuits as of typical motherboard implementation.

Claim 3 is also rejected since the specification also fails to provide supports for the first and second printed circuit board as claimed similarly to the discussion of claim 17 above.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1, 3, and 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, "the data" (line 9) lacks antecedent basis. Correction/clarification required.

Claim 17 recites the first printed circuits connecting to the memory controller and the memory module and a second printed circuit connected to the memory module and the logic. It is unclear if the first and second printed circuits are referred to the memory controller and the memory module or two separate circuit boards in addition to the memory module and the memory controller. It is also unclear how a printed circuit board is connected to a logic.

Claim 3 is also rejected because it is unclear the relationship between the first and second circuit board with respect to the memory controller and the memory module.

Claims 18-20 are rejected because they depend from claim 17.

Correction/clarification required.

9. The following rejections are made based on the examiner's best interpretation of the claims in light of the 35 USC 112 rejection.

Claims 3 and 17 will be interpret that the controller and memory module are implemented as separate printed circuit board as in typical motherboard implementation in view of paragraph 31 of the specification.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-2 and 4 √ are rejected under 35 U.S.C. 102(b) as being anticipated by Jeddeloh et al. (US 6,820181).

Claims 1-2, Jeddeloh discloses a system for responding to requests (Fig. 2) comprising: requesting node (memory controller 110) for transmitting a request (command/request is sent from the memory controller 110 to the memory module 130 via memory controller hub 126, col. 4, ll. 17-22); a responding node (memory module 130) for transmitting a response to the request (data is sent from memory device in response to the request, col. 5, ll. 43-49); and logic (hub controller/hub operation) for transmitting a signal to the requesting node indicating presence of response (read

response 210, col. 5, ll. 64-67), said logic receiving a signal from the responding node indicating the presence of the data (read data signal, col. 5, ll. 43-45) and receiving a signal from the requesting node indicating the presence of the request (memory request signals, col. 4, ll. 17-22) wherein the request is either a read command.

Claim 4, the circuit of claim 2, wherein the memory controller 110 further comprises: a sequencer core (memory request queue 160) for issuing the read command; and a queue 170 for receiving the data.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3, 17 and 20 rejected under 35 U.S.C. 103(a) as being obvious over Jeddeloh in view of applicant's admitted prior art (APA, paragraphs 8 and 31).

As best understood of claims 3 and 17 in light of the 35 USC 112 above, Jeddeloh discloses a circuit for transferring from memory having memeory controller and module as claim (see rejection of claims 1-2 above). Jeddeloh does not explicitly disclose a first and second printed circuits as claimed. However, as admitted by the applicant, it is typical for memory controller and memory module to be implemented as separate integrated circuits on the motherboard to conduct read and write transactions over a printed circuit connecting to the memory module. It would have been obvious to

one having ordinary skill in the art to implement the controller 110 and the memory module 130 as separate printed circuits in typical motherboard integrated circuit implementation in order to take advantage of the available manufacturing process of circuit board.

Claim 20, Jeddeloh discloses the memory controller 110 further comprises: a sequencer core (memory request queue 160) for issuing the read command; and a queue 170 for receiving the data.

14. Claim 10 is rejected under 35 U.S.C. 103(a) as being obvious over Jeddeloh. Jeddeloh discloses the memory module can be SDRAM or any other memory devices except specifying DDR-SDRAM. It would have been obvious to one having ordinary skill in the art to utilize DDR-SDRAM in place of the memory module of Jeddeloh in order to double the memory chips' data throughput and reduce power consumption (inherently advantage of DDR-SDRAM) since Jeddeloh indicates that his device works with all types of SDRAM.

Allowable Subject Matter

15. Claims 18-19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims

16. Claims 5-9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter:

Claims 5 and 18 recite, inter alia, the circuit of claims 2 wherein the logic having an AND gate for transmitting the signal to the memory controller after a time interval, wherein during the time interval, the AND gate receives the signal from the memory controller and the signal from the memory module or circuit of claim 17 wherein the logic having first and second delay logic connected together and an OR and AND gate connected as claimed.

The references of record do not teach or suggest the aforementioned limitation, nor would it be obvious to modify those references to include such limitation.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. (US 6,498,766), Sinclair et al. (US 6,657,634), LaBerge (US 6,763,416), and Murakami (US 6,445,642) disclose various apparatus for controlling DDR-SDRAM.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571) 272-4147.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kim Huynh
Primary Examiner
Art Unit 2182

KH
11/16/04